embodiment, signals d and d# are complementary signals, i.e. complementary of one another, received by the second delay cell **202**, where signals d and d# are the same as delay element output signals $\mathbf{105}_2$. In one embodiment, signals y and y# are complementary signals provided by the first delay cell **201**. The signals y and y# correspond to output signals $\mathbf{105}_2$ from the delay element $\mathbf{104}_1$, and where output signals y and y# are complementary signals with smooth rising and falling edges. In one embodiment, signals y and y# are complementary signals provided to the second delay cell **202** which generates complementary control signals **107**.

[0050] In one embodiment, other inputs to the delay cell **300** are signals including Vbn and Vbp, where signal Vbn is a bias voltage signal for n-type MOS (NMOS) transistors while Vbp is a bias voltage signal for p-type MOS (PMOS) transistors. In one embodiment, the bias signals Vbn and Vbp are generated by a bias generator (not shown). In one embodiment, the bias generator comprises a band-gap circuit. In other embodiments, other forms of bias generators may be used without changing the scope of the embodiments of the invention.

[0051] In one embodiment, a tunable varactor **301** is coupled to the output nodes carrying the signals y and y#. In such an embodiment, the varactor provides a variable capacitance to signals y and y#, where the variable capacitance is a function of the voltage signal, tune. An embodiment of a varactor **301** is described with reference to FIG. **4**. In one embodiment, the delay cell **300** does not have any varactor coupled to the output nodes carrying the signals y and y#.

[0052] In the embodiments discussed herein the delay cell **300** comprises a PMOS differential pair **302** and an NMOS differential pair **303**.

[0053] In one embodiment, the delay cell **300** comprises a PMOS differential pair **302** which comprises PMOS transistors MP**2** and MP**4** that receive differential signals d and d# respectively. A PMOS current source MP**1**, coupled between a power supply and the PMOS differential pair **302**, is biased by Vbn, where MP**1** provides current to the PMOS differential pair **302**. In one embodiment, the power supply is a separate power supply than VH and/or VL which provides the capability to power down the delay cell **300** when a corresponding switch-resistor (for which the control signals y and y# are being generated) is not being used.

[0054] The PMOS transistors MP**2** and MP**4** of the PMOS differential pair **302** are coupled in cascode (in series) with PMOS transistors MP**3** and MP**5** respectively. In one embodiment, PMOS transistors MP**3** and MP**5** are biased by bias voltage Vbp. In one embodiment, the source terminals of the PMOS transistors MP**3** and MP**5** are coupled to output nodes which carry signals y and y# respectively.

[0055] In one embodiment, the NMOS differential pair **303** comprises NMOS transistors MN**7** and MN**9** that receive complementary signals d and d# at their respective gate terminals. In one embodiment, the NMOS differential pair **303** is provided via their source terminals with a current tail source via transistor MN**1** which is biased by Vbn at its gate terminal. In one embodiment, cascode NMOS transistors MN**6** and MN**8** are coupled in series with the NMOS differential pair **303** transistors MN**7** and MN**9** respectively. In one embodiment, the cascode NMOS transistors MN**6** and MN**8** are biased by the bias signal Vbn which is coupled to their gate terminals. In one embodiment, the drain terminals of the NMOS cascode transistors MN**6** and MN**8** are coupled to output nodes which carry signals y# and y respectively.

[0056] In one embodiment, a pair of NMOS transistors MN**2** and MN**3**, which are coupled together in series, couple the drain terminal of the PMOS current source MP**1** and the output node carrying the signal y, such that the source terminal of MN**3** is coupled to the output node carrying the signal y, and the drain terminal of MN**2** is coupled to the drain terminal of the PMOS current source MP**1**, wherein the pair of NMOS transistors MN**2** and MN**3** receive the input signal d at their respective gate terminals.

[0057] In one embodiment, a pair of NMOS transistors MN**4** and MN**5**, which are coupled together in series, couple the drain terminal of the PMOS current source MP**1** and the output node carrying the signal y#, such that the source terminal of MN**5** is coupled to the output node carrying the signal y#, and the drain terminal of MN**4** is coupled to the drain terminal of the PMOS current source MP**1**, wherein the pair of NMOS transistors MN**4** and MN**5** receive the input signal d# at their gate terminals.

[0058] In this embodiment, transistors MN**2**, MN**3** and MN**4**, MN**5** are operated as source-followers to enhance the linearity of the waveforms of the signals y and y#. Coupling the two transistors (MN**2**, MN**3** and MN**4**, MN**5**) in series emulates a long-channel transistor device. A person skilled in the art is aware of the benefits a long-channel transistor as used in analog design.

[0059] In one embodiment, a pair of PMOS transistors MP**6** and MP**7**, which are coupled together in series, couple the drain terminal of the NMOS tail current source MN**1** and the output node carrying the signal y, such that the drain terminal of MP**6** is coupled to the output node carrying the signal y, and the source terminal of MP**7** is coupled to the drain terminal of the NMOS tail current source MN**1**, wherein the pair of PMOS transistors MP**6** and MP**7** receive the input signal d at their gate terminals.

[0060] In one embodiment, a pair of PMOS transistors MP**8** and MP**9**, which are coupled together in series, couple the drain terminal of the NMOS tail current source MN**1** and the output node carrying the signal y#, such that the drain terminal of MP**8** is coupled to the output node carrying the signal y#, and the source terminal of MP**9** is coupled to the drain terminal of the NMOS tail current source MN**1**, wherein the pair of PMOS transistors MP**8** and MP**9** receive the input signal d at their respective gate terminals. The differential delay cell **300** of FIG. **3** generates differential output signals y and y# having the same rise and fall slopes which are smooth, i.e. not stair case.

[0061] In one embodiment, transistors MP**6**, MP**7** and MP**8**, MP**9** are operated as source-followers to enhance the linearity of the waveforms of y and y#. Coupling the two transistors (MP**6**, MP**7** and MP**8**, MP**9**) in series emulates a long-channel transistor device. In one embodiment, transistors MP**6**, MP**7** and MP**8**, MP**9** may be removed.

[0062] In one embodiment, the slew rate of the controls signal **107**, i.e. signals y and y#, increases when tune signal level is increased and/or when Vbn voltage level is increased and Vbp voltage level is reduced. In such an embodiment, Vbp is indirectly controlled by a bias current provided by transistors MN**1**/MP**1** which are part of current mirrors. As the slew rate of signals y and y# increases, i.e. slew rate of control signal **107**, the delay from signals d/d# to y/y# is reduced, which results in higher frequency.